PRODUCT FACT SHEET

Horizon Robotics

HORIZON JOURNEY™ 5 Automotive Processor

Efficient Computing at the Edge to Redefine Automated Driving

Optimized Edge Processor for Automotive Intelligence

Assisted and autonomous driving systems face real-time computation challenges today to deliver high performance at low latency, while maintaining high energy efficiency and high-cost effectiveness for perception, fusion, localization, planning and control tasks.

Following Journey 3, the Journey 5 processor harnesses the full potential of accelerated computing to meet this challenge, with Horizon Robotics' highly efficient, domain specific compute architecture.

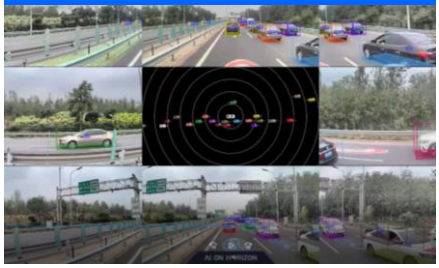
Journey 5's accelerator consists of two cutting-edge Brain-Processing Unit cores, or BPU™. Enabled by fully optimized scenario-based algorithms and an easy-to-use toolkit, Journey 5 is built to deliver environmental perception, fusion, localization, mapping, prediction and planning in a multi-sensor environment.

Journey 5 offers over 20 different cores to meet automotive specific workload requirements, including the dual-core BPU, an Octa-core ARM Cortex CPU, two DSP cores, two ISP engines, a CV engine with Optical Flow and Pyramid, a video encoder/decoder, a crypto engine and two lockstep MCUs in a safety island. Journey 5's heterogenous architecture delivers an optimal mix of flexibility and efficiency.

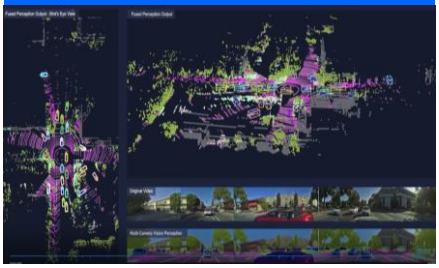
To meet automotive quality and safety requirements, Journey 5 was designed under certified standards and processes of AEC-Q100 Grade 2, ASPICE CL2 and received ISO-26262 ASIL B certification.

128 Performance TOPS	**A55** Octa-Core CPU
1,737 FPS FCOS EffNet	**2x GbE CAN FD**
Open SW Toolkit	**DSP** Software Flexibility
ASIL-B	Horizon Robotics Journey™ 5

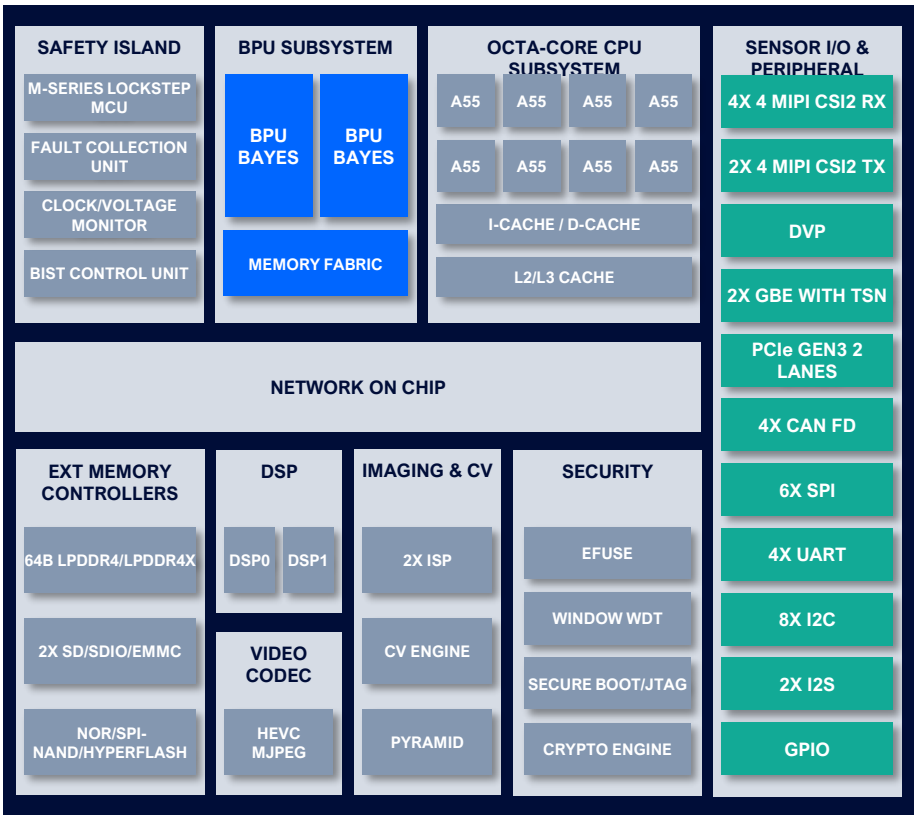
Multi-camera perception

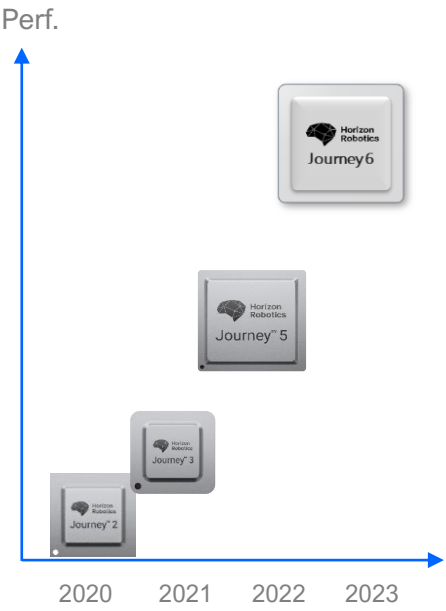


Vision and LiDAR fusion



Urban NOA





KEY FEATURES

CPU Processor Cores	▪ Octa-Core ARM Cortex® A55 up to 1.2 GHz ▪ 32KB L1 I-cache, 32KB L1 D-cache ▪ 128KB L2 cache, 2MB L3 cache ▪ ECC/Parity protection
Brain Processing Unit	▪ Dual core BPU Engine based on Bayes Architecture ▪ Up to equivalent 128 TOPS ▪ Fully optimized for ADAS and AV driving scenario
Image Processing	▪ Two ISP for superb performance, up to 2x4K per ISP ▪ Multi-exposure HDR with pixel tone mapping. Multi camera support ▪ Flexible CFA support: RGGB, RCCC, RGBIR, RCCB, RCCG, RYYCy
Pyramid	▪ Up to 2x4K per Pyramid module ▪ YUV422/420 input. 6-channel downscaling output for programmable ROI
DSP	▪ Two programmable DSP processors for CV acceleration and deep learning flexibility
Video codec	▪ HEVC/MJPEG 4K video codec
Camera interface	▪ RX: Four MIPI-CSI host controllers with D-PHY. 2.5Gbps per lane, 16 lanes/40Gbps ▪ TX: Two MIPI-CSI device controllers with D-PHY. 2.5 Gbps per lane, 8 lanes/20Gbps
Peripherals	▪ Dual Gigabit Ethernet (RGMII) with PTP/AVB-TSN ▪ Dual PCIe Gen3 for high-speed data exchange between processors ▪ Quad CAN FD for radar and car network
Safety and Security	▪ Target ISO 26262 ASIL B. Comprehensive coverage for single point and latent faults ▪ Safety island with dual lockstep MCU cores. Fault collection and handling module ▪ ARM Trustzone. Secure boot and crypto engine. Memory protection. Key management
SW Toolkit	▪ Optimize and deploy algorithms on Journey 5 ▪ Support quantization aware training and post-training quantization of ONNX model ▪ Training, quantization, automatic compiler optimization, deployment (SDK) ▪ Design examples and best practices to achieve short time-to-market